portion of data and the second portion of data are included in the same packet].

159. (Amended) The method of claim 158 wherein the write request is included in a first packet, and the first portion of data and the second portion of data are included in a second packet.

160. (Amended) The method of claim 158 wherein the write request includes an operation code[, the first portion of data and the second portion of data are included in the same packet].

Kindly **ADD** the following claims:

-- 176. A method of controlling a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

providing first block size information to the memory device, wherein the first block size information defines an amount of data to be input by the memory device in response to a write request;

issuing the write request to the memory device, wherein the memory device samples the write request synchronously with respect to an external clock and, in response to the write request, the memory device samples first and second portions of data;

providing a first portion of data to the memory device synchronously with respect to a rising edge transition of an external clock signal; and

providing a second portion of data to the memory device synchronously with respect to a falling edge transition of the external clock signal.

177. The method of claim 176 wherein the write request is included in a first packet and both the first and second portions of data are included in a second packet.

178. The method of claim 176 wherein the write request includes an operation code.

179. The method of claim 178 wherein the memory device samples the operation code synchronously with respect to a first transition of the external clock signal.

180. The method of claim 176 wherein:

a first portion of the amount of data is sampled by the memory device in response to a rising edge transition of the external clock signal; and

a second portion of the amount of data is sampled by the memory device in response to a falling edge transition of the external clock signal.

181. The method of claim 176 wherein the first block size information and the write request are included in a packet.

182. The method of claim 176 further including:

providing second block size information to the memory device, wherein the second block size information defines an amount of data to be output by the memory device in response to a read request;

issuing a first read request to the memory device; and

receiving the amount of data output by the memory device.

183. The method of claim 176 further including providing access time information to the memory device, wherein the access time information is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs data.

184. The method of claim 176 further including providing the external clock signal to the memory device wherein:

in response to a first edge transition of the external clock signal the memory device samples the first portion of the data; and

in response to a second edge transition of the external clock signal the memory device samples the second portion of the data, wherein the first and second edge transitions are from the same clock cycle of the external clock signal.

185. The method of claim 176 wherein the external clock signal is provided by an external clock generator.